

III. REMARKS

Claims 15, 44 and 45 are rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 has been amended to recite the relationship of the filtering operation to the basic processing elements. Claim 44 has been cancelled. Claim 45 has been amended to relate the core processing unit to the basic processing stages. It is therefore submitted that claims 15 and 45 conform to 35 USC 112, second paragraph.

Claim 1-5,12, 15, 16, 20-25, 27, 40, 41 and 43-45 are rejected under 35 USC 102(e) as being anticipated by Turney.

The Examiner states:

Turney's Fig 6 clearly shows a microprocessor structure (inverse discrete wavelet packet) for performing a discrete wavelet transform

It is respectfully submitted that in making this statement, the Examiner is mixing together different concepts. The first paragraph of the specific description of Turney (column 2, lines 59 to 67) states:

For many wavelet systems, a single stage is insufficient. Thus, a wavelet tree structure including multiple instances of a single stage wavelet structure is usually employed. The interconnection of the single stage wavelet structures in a multi-stage implementation gives rise to three fundamental structures: the Discrete Wavelet Transform (DWT), the Discrete Wavelet Packet (DWP), and the Custom Wavelet Tree

(CWT). The DWT, DWP, and CWT have different applications as known in the art.

Clearly, this section of Turney is stating the DWTs and DWPs are different. This is explained in more detail further on in this reference, for example at column 3, lines 1 to 12, a DWT is described:

FIG. 1A is a block diagram of a three-stage forward DWT arrangement, and FIG. 1B is a block diagram of a three-stage inverse DWT arrangement. The DWT terminology refers to a wavelet transform that has a tree structure where the low pass components are passed and split in each level of the tree while the high pass components are provided as output data. This results in a logarithmic division of the frequency domain. For n levels of a forward DWT, the output data stream includes every other output from stage 1, every fourth output from stage 2, every eighth output from stage 3, . . . , and every $2^{\text{sup.}n}$ output from stage n . This same data format is used as input to the Inverse DWT operation.

While at column 4, lines 34 to 39, a DWP is explained:

FIG. 4A is a functional block diagram of a forward DWP arrangement 202. In a forward DWP arrangement, the wavelet transform has a tree structure where both the low and the high-pass components are split in each level of the tree. This results in a uniform division of the frequency domain.

Therefore, this reference explains how a DWT and a DWP are different and presents functional block diagrams in Figures 1A and 1B (DWT and inverse DWT) and Figures 4A and 6 (DWP and inverse DWP) to illustrate the difference.

Claim 1 relates to a microprocessor structure for performing a discrete wavelet transform operation having the feature that the number of basic processing elements implemented in a number of processing stages decreases by a constant factor at each increasing decomposition level j . The cited figure 6 of Turney relates to an inverse discrete wavelet packet and so naturally does not disclose a DWT but instead discloses a DWP. Therefore, claim 1 is novel over Turney.

Thus the rejection of claims 1-5, 12, 16, 20-25, 27, 40, 41, 43 and 45 under 35 USC 102 on Turney should be withdrawn.

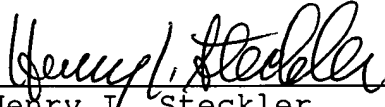
Claim 1 is also inventive over Turney. In particular a DWT is different from a DWP and has a different underlying structure as can be seen by comparing Figures 1A and 1B to Figures 4A and 6. Because the underlying structures define how the DWTs and DWPs operate and impose conditions on how they can be implemented physically as a processing architecture, elements of the structures cannot be interchanged arbitrarily without having an impact on the way they can be realised as a physical processing architecture. Therefore, in the absence of clear reasoning providing guidance on what should be done and exactly how it should be done, arbitrary combinations of features taken from DWTs and DWPs are not obvious. Applying this reasoning to the case of the present application, it would not be obvious to take the feature that the number of basic processing elements implemented in each of a number of processing stages decreases by a constant factor at each increasing decomposition level j from an inverse DWP and include it in a DWT. Doing this would change the nature of the DWT and lead to unforeseen consequences unless these had been analysed and dealt with beforehand. Since Turney includes no such teaching, a discrete wavelet transform operation

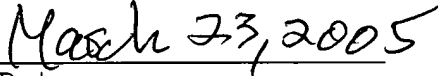
having the feature that the number of basic processing elements implemented in each of a number of processing stages decreases by a constant factor at each increasing decomposition level j is not obvious in an architecture for performing a DWT because there is no indication in Turney that this feature could be included and, more importantly, how it should be implemented to provide a working DWT.

For all of the foregoing reasons, it is respectfully submitted that all of the claims now present in the application are clearly novel and patentable over the prior art of record, and are in proper form for allowance. Accordingly, favorable reconsideration and allowance is respectfully requested. Should any unresolved issues remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

A check in the amount of \$1,020.00 is enclosed for a 3 month extension of time fee. The Commissioner is hereby authorized to charge payment for any fees associated with this communication or credit any over payment to Deposit Account No. 16-1350.

Respectfully submitted,


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